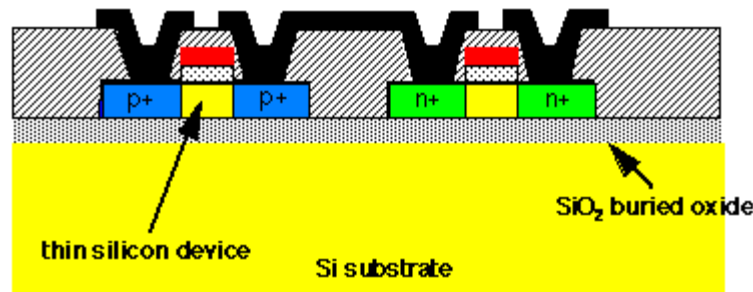


Evaluation of Silicon on Insulator (SOI) Processes for Mixed Signal ASICs



- **Scope:**
- Design of process evaluation and transistor reliability test structures
- Target CMOS/SOI technologies:
 - 0.8-um and 0.35-um, partially depleted
 - 0.25-um, 0.18-um, and 0.1-um, fully depleted
- Fabrication by Honeywell and Lincoln Lab
- Design of parametric tests and Hot-Carrier stress tests
- Tests at temperatures down to -150°C
- Process qualification reports [GSFC]
- Collaborate with CISM/SOAC program to provide critical information for circuit designers

Objective:

- Perform a comprehensive technology characterization of SOI processes in partnership with industry, academia, and government-sponsored laboratories. Provide critical information for design engineers and circuit designers relating to the characteristics and limitations of this technology for high reliability applications in an extended temperature range down to -150°C .

Status:

- 2-year task initiated in FY '00

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